Anish Rajesh

EDUCATION & HONORS

University of Illinois Urbana-Champaign | B.S. Electrical Engineering w/ Honors | Dean's List **2020-2024**
University of California Los Angeles | M.S Electrical Engineering, Online **2026 - Expected 2028**

SUMMARY

Senior Physical Design Application Engineer with 2+ years supporting enterprise PnR customers at Cadence. Strong foundation in Innovus place-and-route, timing closure, clock network design, PPA optimization, and full-flow PnR ownership from RTL through GDSII.

SKILLS & FRAMEWORKS

Skills: Place & Route, STA, PPA Optimization, Python, Tcl, Verilog/SystemVerilog, C/C++, Pandas, Matplotlib, Numpy
Tools: Quartus Prime, Synopsys FineSim, Cadence Virtuoso/Genus/Innovus & InnoStack+, Git, JIRA

COURSEWORK & SELF-DIRECTED STUDY

Coursework: Digital Systems Lab (RTL/FPGA), Analog IC Design, VLSI Design, Senior Design Lab
Self-Directed Study on PD topics: Timing closure scenarios on customer design, low-power flows, SV/RTL Design

WORK & EXPERIENCE

Cadence Design Systems | *Senior Physical Design Application Engineer – San Jose, CA* **June 2024 - Present**

- Partnered with enterprise CPU/SoC customers on 10+ tapeout-critical PnR challenges in Innovus; debugging timing violations, congestion hotspots, power-grid issues, and signoff blockers across advanced-node designs.
- Engineered 5+ Tcl/Python automation scripts to parse timing reports, power data, and congestion metrics from PnR runs, streamlining backend physical design analysis and reducing report generation time by 40%.
- Drove resolution of 7+ critical PnR issues (timing closure, routing congestion, DRC violations) by deep-debugging customer designs alongside R&D, contributing to ~15% PPA improvement and faster tapeout convergence.
- Contributed to flow and methodology improvements that streamlined customer PnR debug cycles; applying CAD-style thinking (automated data analysis, flow recommendations, methodology development) across multiple advanced nodes.

Cadence Design Systems | *Physical Design Application Engineer Intern – San Jose, CA* **May 2023 - Aug 2023**

- Led migration of 2 digital blocks of a sous vide controller from 45nm to SkyWater 130nm; closed timing from -2.3ns to +0.15ns slack at ~64 MHz target frequency, with final area ~29,800 μm² and ~2.77 mW power.
- Adapted Tcl scripts, LEF/Tech LEF files, and RTL across Cadence Genus and Innovus to enable full synthesis + PnR flow execution on an open-source PDK with incomplete collateral; hand-fixing library views to unblock place-and-route.
- Aligned analog and digital teams to integrate 2 black-box macros into the PnR flow, supporting final backend delivery to senior leadership.

Analog Bits | *Application Engineer Intern - Sunnyvale, CA* **May 2022 - Aug 2022**

- Conducted burn-in tests on **90+ test-chips for 3 integrated circuit IPs** according to IEEE and JEDEC industry standards, analyzing silicon performance (process, voltage, jitters) to support silicon validation and customer signoff.
- **Developed 8+ python scripts to interface with lab equipment** via the PyVisa SCPI library and generate MATLAB performance plots, enabling efficient analysis of silicon metrics and customer-facing debug.
- **Generated 150+ waveforms and ran simulations** to evaluate IP characteristics (phase noise, jitter) using Mentor Graphics' EZwave EDA tool, supporting signal integrity analysis and validation of design behavior.

PROJECTS

ChipCaddy | ECE 445: Senior Design Lab

- Designed a microcontroller-based system supporting 20+ chips with custom digital control logic for pot tracking and multi-way split, with STM32 firmware programmed via STMduino + SWD.
- Completed full PCB schematic, layout, and routing across 7+ components; led team in soldering and validating 2+ board prototypes before firmware integration.

LEADERSHIP & INVOLVEMENT

Medium Blog Page | ***Writer – (medium.com/@anish.rajesh)***

- Author of technical articles on integrated circuit applications, Moore's Law trajectory, and emerging EDA challenges at advanced process nodes, including how AI is reshaping the EDA toolchain.

Boy Scouts of America Troop 40 | *151st Eagle Scout – Princeton Junction, NJ*

- Directed 20+ volunteers in completing a park construction project from concept to execution, culminating a 9-year scouting career.